IEEE Guide on Electrostatic Discharge (ESD): ESD Withstand Capability Evaluation Methods (for Electronic Equipment Subassemblies)

Sponsor

**Surge-Protective Devices Committee
of the
IEEE Power Engineering Society**

Approved October 24, 1994

IEEE Standards Board

Abstract: This guide establishes test methods for the evaluation of ESD withstand capability for electronic equipment subassemblies. It includes information about test conditions, test equipment, and test procedures for ESD tests of printed circuit boards and other subassemblies.
Keywords: electronic equipment subassemblies, electrostatic discharge, ESD, subassemblies, withstand capability

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The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

ISBN 1-55937-471-3

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Introduction

[This introduction is not a part of IEEE Std C62.38-1994, IEEE Guide on Electrostatic Discharge (ESD): ESD Withstand Capability Evaluation Methods (for Electronic Equipment Subassemblies).]

Electrostatic discharge (ESD) is one of the prime causes of failure for electronic products. To reduce the level of failures caused by ESD, a two-step design cycle has evolved. The first step is to design the product in a manner that will tend to result in acceptable ESD immunity. The second step involves the use of simulated ESD to test whether the resulting product actually has acceptable ESD immunity for its intended application.

Standardized tests already exist to assess the sensitivity of components, such as integrated circuits (ICs), for ESD. Tests also exist to determine the level of ESD immunity that may be expected for completed equipment. Using such tests, IC designers and equipment designers are able to determine the ESD immunity.

However, a product does not exist only as a collection of separate components or as completed and functioning equipment. Likewise, the ESD threat is not limited to these two states. For example, electronic subassemblies, such as printed-circuit-board (PCB) assemblies, are subjected to ESD during handling by humans, just like ICs.

Since no generic standard ESD tests have existed for subassemblies, designers have had no method to indicate whether their subassembly designs can successfully survive the ESD events to which they are subjected. This guide was developed to provide standardized ESD tests covering subassemblies.

It is not the intent of this guide to imply or require that all electronic equipment subassemblies should be tested for ESD withstand capability.

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IEEE Guide on Electrostatic Discharge (ESD): ESD Withstand Capability Evaluation Methods (for Electronic Equipment Subassemblies)

1. Overview

1.1 Purpose

The purpose of this guide is to define test methods to evaluate the electrostatic discharge (ESD) withstand capability of finished subassemblies that have not been incorporated into the next higher-level assembly.

Test methods are defined to evaluate the ability of such subassemblies to withstand ESD that occurs due to handling, shipping, and installation. These environments may not necessarily be ESD-controlled environments. Some typical electronic subassemblies are populated printed circuit boards, circuit packs, power supplies, plug-in modules, and disk drives.

1.2 Scope

The test methods described are intended to be used to discover subassembly failures that result from destructive ESD, as well as those failures that may result from modification of data stored in subassemblies [e.g., in nonvolatile memory elements such as electronically erasable programmable read-only memory (EEPROM) or battery supported random access memory (RAM)].

This guide does not specify ESD tests to characterize the withstand capability of subassemblies that are incomplete (e.g., in the process of being manufactured), nor the expected ESD immunity of externally powered and/or installed subassemblies. Also, this guide does not specify tests for completed equipment or systems, whether powered or not, nor does it specify ESD tests for individual electronic components, such as integrated circuits. Such ESD tests are covered in other standards (see IEC Pub 801-2 (1991), [B1],[1] [B2], and [B4]).

[1]The numbers in brackets correspond to the bibliographical items listed in clause 9.

2. Reference

This guide shall be used in conjunction with the following publication:

IEC Publication 801-2 (1991), Electromagnetic compatibility for industrial-process measurement and control equipment—Part 2: Electrostatic discharge requirements.[2]

3. Definitions

3.1 air discharge method: A method of ESD testing in which the charged electrode of the ESD simulator approaches the Unit Under Test (UUT) or coupling plane. The discharge is actuated by a spark in the air to the UUT or to the coupling plane.

3.2 circuit pack: A printed circuit board (PCB) populated with components, i.e., a PCB assembly. Also called a feature card.

3.3 contact discharge method: A method of ESD testing in which the electrode of the ESD simulator is in firm conductive contact with the UUT or coupling plane prior to and during the discharge. The discharge is actuated by a switching device, such as a relay, within the simulator.

3.4 ESD simulator ground: The pulse-current return connection of the ESD simulator.

3.5 failure: The termination of the capability of the subassembly to perform its required function.

3.6 subassembly: Items that have an identifiable function. Subassemblies are not completed equipment or individual components.

4. Safety

Although the energy involved in ESD tests is generally not considered hazardous, ESD tests do involve high voltages and generate significant fields. Therefore, common sense dictates certain safety precautions.

a) Do not perform tests near personnel with electronic life support items, such as pacemakers or insulin injection systems.

b) Do not test near robotic equipment or other machinery that may become dangerous if control is disrupted.

c) Do not test near explosive items or in a potentially explosive atmosphere.

d) Do not perform tests if either the test equipment or the UUT seems to be operating in an unusual manner, or if the laboratory conditions are not properly controlled (that is, if condensing humidity exists).

e) Follow all operational and safety instructions provided by the test equipment manufacturers.

[2]IEC publications are available from IEC Sales Department, Case Postale 131, 3 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse. IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

5. Laboratory conditions

5.1 Climate conditions

The ESD tests described in this guide should be performed under the following climatic conditions:

Temperature: 15–35 ˚C
Humidity: 30–60%
Atmospheric Pressure: 68–106 kPa

NOTE—Standard conditions are defined as101.3 kPa and at 15 °C at sea level. Thus, 106 kPa is equal to –383 m and 68 kPa is equal to +3236 m altitude. International conversion for 1 kPa is 0.145 psi, or 0.2953 in Hg (typical reported atmospheric pressure measurement in the US), or 10 mbar.

5.2 Electromagnetic conditions

The ambient electromagnetic conditions should be such that they do not influence the results of the test.

6. Test methods

The ESD events that will be covered by this guide are

a) Body/Finger (also known as human body model)
b) Hand/Metal

See also IEC Pub 801-2 (1991), [B2], [B5], [B6], [B7], and [B8].

There are two associated test methods to verify the ability of the subassembly to withstand ESD in these two cases. Details common to these test methods are included in 6.1 and 6.2. Subclause 6.3 provides details specific to the simulation of personnel ESD.

To determine which of the two ESD test methods are appropriate for a specific subassembly, it is necessary to evaluate the handling, shipping, and installation practices for the subassembly. As indicated in figure 1, the type of contact with personnel will determine the test method that should be used. It is virtually impossible to ensure that subassemblies will not be subjected to any ESD. Therefore, the decision is usually which ESD test method to use, not whether to test or not (see [B2]).

Personnel ESD waveforms are broken down into two categories. One is body/finger (also known as human body model) and the other is hand/metal.

Body/Finger ESD simulates a person discharging stored charge from their finger to the subassembly. An example of this is a discharge that occurs when a person picks up or touches the subassembly.

Hand/Metal ESD simulates a person discharging stored charge through a metal object to the subassembly. An example of this is a discharge that occurs when a person contacts the subassembly through a ring or a metal tool.

6.1 Configuration of the unit under test (UUT)

The UUT should be tested in the normal configuration that would exist for production units. Shipping materials and/or protective covers used in shipping should be removed during ESD testing.

6.2 General test requirements

Three discharges of simulated ESD in both polarities should be applied to each test point (see [B4]). If metallic contact with the UUT is possible, contact mode ESD is preferred for repeatability (see figure 2). If metallic contact with the UUT is not possible, then air discharge may be used. Though contact mode ESD can achieve a higher degree of repeatability, air discharge mode ESD offers a closer representation of reality. Contact discharge and air discharge may not have equivalent results. The rate at which the discharges are applied to the UUT should not exceed once per second in order to prevent charge buildup or accumulated heating effects. It is recommended that multiple test voltage levels be used in order to verify that there are no intermediate levels at which the ESD protection is not effective.

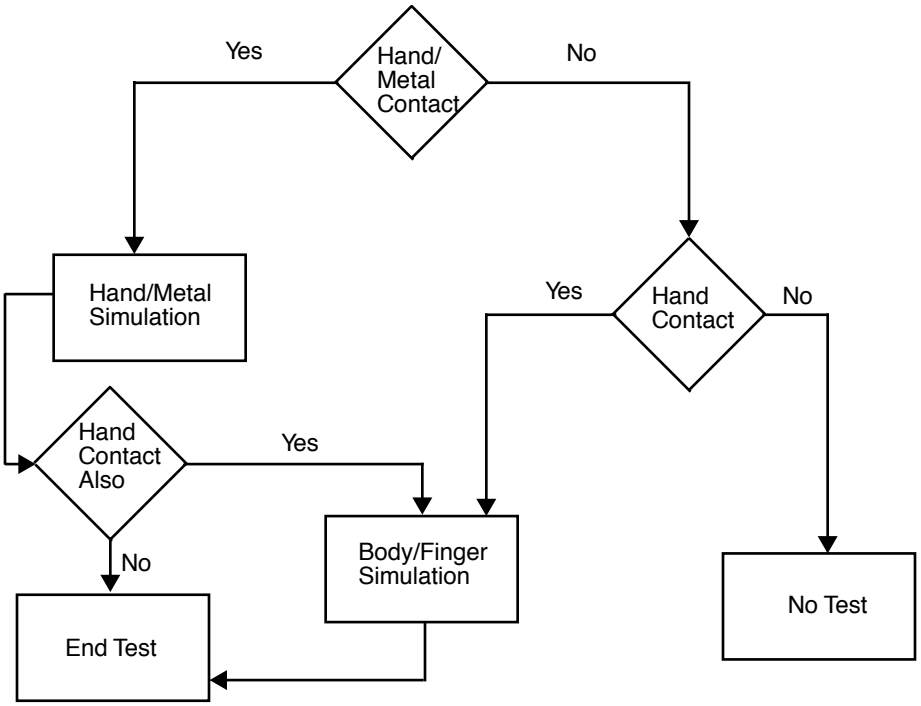


Figure 1—Appropriate test methods for different possible threats

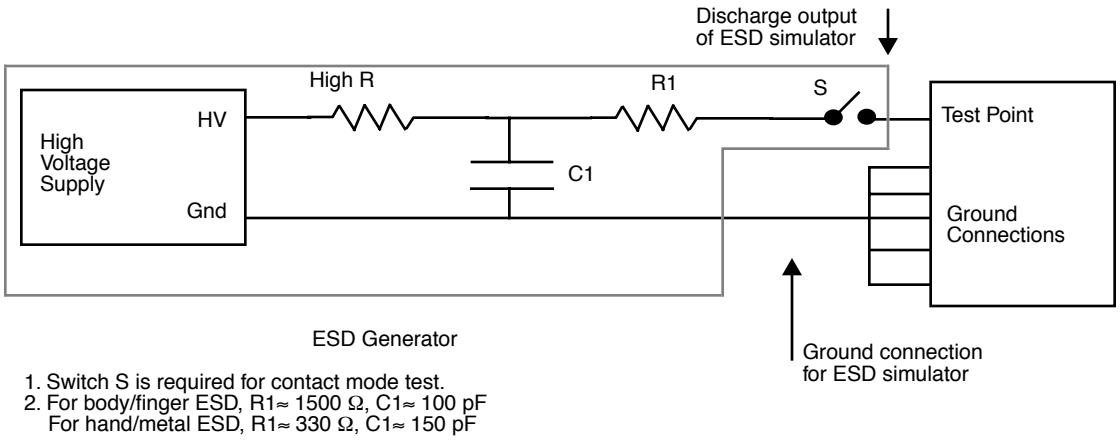
6.2.1 Test points

In the absence of a set of agreed test points, the following ESD test points are recommended:

— Subassembly connector pins
— Subassembly circuit test points
— Accessible pins of components
— Permanently attached leads or cables
— Other likely points of ESD entry into the subassembly

6.2.2 Bleeding off trapped charge

To prevent charge from being trapped on or in the UUT, and thereby reducing the effective stress level, any conductive area of the UUT that is isolated from ground, and which has simulated ESD applied, should be connected to the ESD simulator ground via a bleed path incorporating a 1 MΩ (±50%) resistor at each end. This bleed path will not affect the results of the test and may be left connected during the application of ESD. A 2 kΩ resistor should be connected in series with the 1 MΩ resistor located near the ground end of



1. Switch S is required for contact mode test.
2. For body/finger ESD, R1≈ 1500 Ω, C1≈ 100 pF
   For hand/metal ESD, R1≈ 330 Ω, C1≈ 150 pF

NOTE—Conceptual representation only. Circuit construction may vary in order to achieve proper representation. In particular, free-space capacitance may be required.

Figure 2—Simplified personnel ESD simulation circuit diagram

the bleed path [see IEC Pub 801-2 (1991)]. If a bleed path is not feasible, then some other means, such as ionized air, should be used to bleed off trapped charge from isolated conductive areas.

NOTES

1—Ionizers may require significant time to remove charge. If ionizers are used, the subassembly charge level should be verified to ensure the charge voltage that remains on the UUT is no more than 1% of the test voltage or 50 V, whichever is greater. This should be done by using a noncontacting, chopper stabilized voltmeter.

2—The 1 MΩ resistor located at each end of the charge bleed path should have a withstand voltage greater than half of the applied ESD voltage. The high voltage requirement is necessary to prevent breakdown current from creating false current loops. The 2 kΩ resistor prevents the stray capacitance of the high voltage resistor from forming a ringing circuit with the inductance of the ground lead.

6.3 Simulation of personnel ESD

The procedure to simulate body/finger ESD is the same as for hand/metal ESD (see figure 2). In both cases, the following connection schemes should be considered:

a) All subassembly grounds (e.g., analog, digital, etc.) are connected to the ESD simulator ground while the simulated ESD is applied to the selected test points, one at a time;
b) All subassembly power connections (e.g,. +5 V, –12 V, etc.) are connected to the ESD simulator ground while the simulated ESD is applied to the selected test points, one at a time;
c) Ground connections of the same type are connected as a group to the ESD simulator ground while simulated ESD is applied to grounds of other types and all power connections (e.g., connect analog grounds together and apply ESD to the digital ground);
d) Power connections of the same type are connected as a group to the ESD simulator ground while the simulated ESD is applied to each other power connection of other types and all grounds, one at a time (e.g., connect all +5 V power connections together and apply ESD to the +12 V power connections); and
e) All subassembly connections are left unterminated while the simulated ESD is applied to each test point, one at a time. If this scheme is chosen, the proximity of the ground plane to the subassembly should be documented and the charge should be removed after each discharge, as described in 6.2.2.

6.3.1 Body/Finger ESD simulation

The body/finger ESD simulator concept is based on MIL-STD 883D [B4] and ANSI/EOS/ESD-S5.1-1993 [B1].

6.3.2 Hand/Metal ESD simulation

The hand/metal ESD simulator concept is based on IEC Pub 801-2 (1991). Thus, in contact mode a metallic connection is made and in air discharge a hemispherical tip with an 8 mm diameter is used.

6.3.3 Voltage levels

This guide does not define pass/fail test voltage levels.

In the absence of special requirements, the following test voltage levels are recommended for air discharge or contact discharge:

500 V
1000 V
2000 V
4000 V
6000 V
8000 V

For information about threat levels in the environment, see IEEE Std C62.47-1992 [B2].

7. Test criteria and reports

7.1 Failure definitions and categories

The failure categories that are generally of interest are as follows:

— *Nonrecoverable*: Damage to components or permanent loss of data. The subassembly has to be repaired to restore operation.

In some cases, the following categories are also considered failures:

— *Operator intervention*: An operator is required to restore the subassembly to functional specifications (e.g., reloading a program into memory).
— *Automatically recoverable*: Errors that require no operator intervention to correct (e.g., redundant circuitry may allow correct operation in spite of failure of part of the subassembly).

7.2 Establishing withstand capability level

The withstand capability level of the UUT is the maximum voltage level below which failure does not occur. To determine whether failure has occurred, the subassembly should be functionally tested before and after the application of simulated ESD at each selected voltage level. The performance of the subassembly should meet the full data sheet specifications. If not, the subassembly has failed and can be described as one of the failure categories in 7.1.

7.3 Test data records

The information in the following subclauses is suggested to be appropriate for data records of the ESD tests outlined in this guide (see [B6]).

7.3.1 UUT information

To ensure reproducible test results, the model number, serial number, revision level, and configuration of the specific UUT tested should be recorded.

7.3.2 Laboratory data

As a control measure, the date, time, and climate conditions should be recorded, as well as the name of the operator performing the test.

7.3.3 Simulator information

Information should be included about the specific simulator. The record should include the exact simulation method used (e.g., hand/metal) and the mode in which it is used (e.g., contact mode). This record should also include the name of the simulator manufacturer, the model number, the serial number, and the last calibration date.

7.3.4 Response data

The response data should clearly indicate the exact UUT response to simulated ESD. For each UUT response, record the following: test voltage level, polarity(s), test point(s), and specific connections made between the subassembly and the ESD simulator.

8. Performance specifications and verification procedures for ESD simulation equipment

8.1 Personnel ESD simulation equipment

To achieve the specified waveform, as described in the following subclauses, contact mode ESD is required.

8.1.1 Body/Finger ESD simulation

Verification of the performance of the body/finger simulator is based on the current waveform of the simulator discharging into two different loads (see figure 3). A current probe with a bandwidth greater than 350 MHz is used to measure the current waveform in each of two loads.

The current probe is placed at the point at which the ESD simulator would have injected current into an actual UUT. The waveforms should meet the requirements of tables 1 and 2 and figures 4–6. Also, there should be no transients after the waveform, either positive or negative, whose peak values exceed 10% of the peak amplitude of the waveform itself.

To measure these waveforms, an oscilloscope with a minimum bandwidth of 350 MHz is used. The oscilloscope should be capable of accurately measuring all the parameters required for the waveforms, including ringing. The 500 Ω resistor is used only for tests at 1 kV. An appropriate resistor for this test is one with minimal series inductance. The tolerance of the resistance is less than 1%.

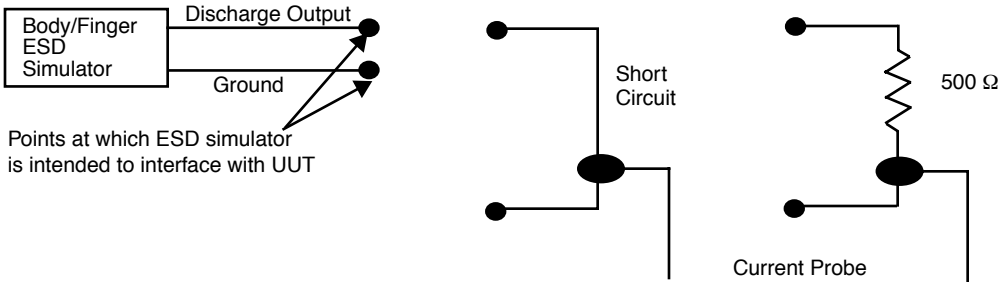
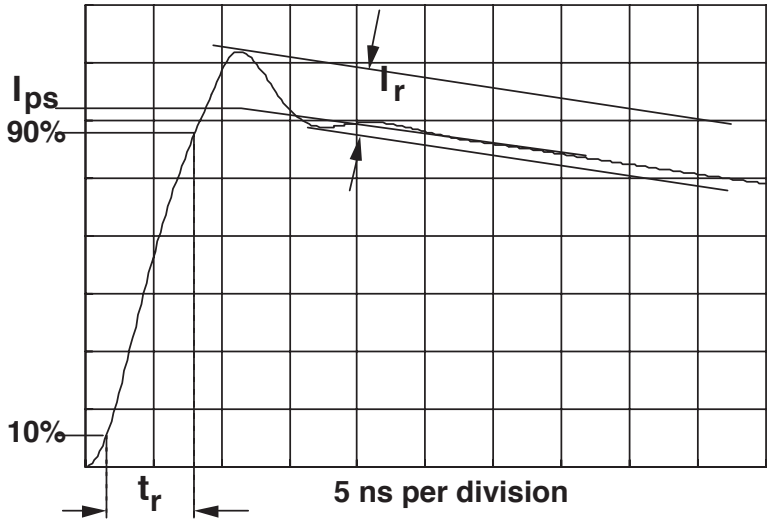


Figure 3—Waveform verification for body/finger ESD simulator



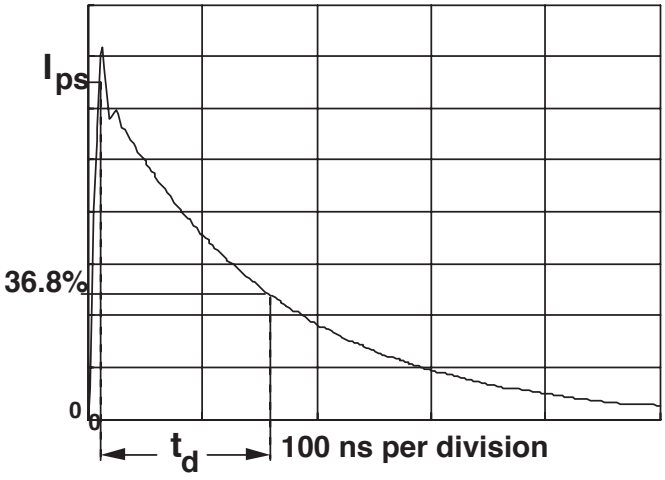
NOTES
1—The maximum allowable peak-to-peak ringing has to be less than 15% of I_{ps} with no observable ringing 100 ns after the start of the pulse.
2—Peak current (I_{ps}) shall be within 10% of the values specified in table 1. The actual values obtained have to be recorded for comparison with the I_{pr} values obtained with the 500 Ω resistor.

Figure 4—Current waveform through a short (T_{rs})

8.1.2 Hand/Metal ESD simulation

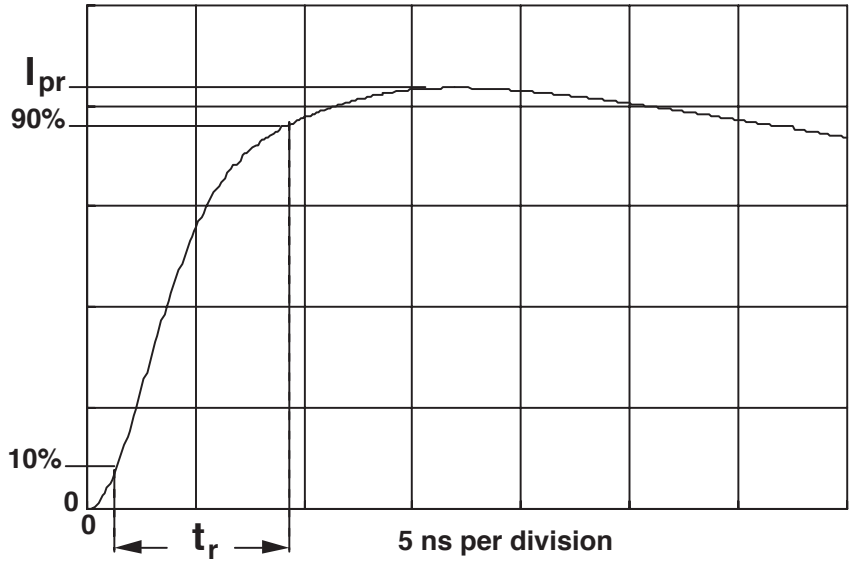
Verification of the performance of the hand/metal simulator is based on the short-circuit current waveform of the simulator (see figure 7). A current viewing resistor (CVR), as specified in IEC Pub 801-2 (1991), is used. The CVR is placed at the point at which the ESD simulator would have injected current into an actual UUT. The waveform should meet the requirements of table 3 and figure 8. This guide does not specify air discharge waveform parameters. Also, there should be no transients after the waveform, either positive or negative, which exceed 15% of the amplitude of the waveform itself.

To measure these waveforms, an oscilloscope with a bandwidth of 1 GHz should be used. The oscilloscope should be capable of accurately measuring all the parameters required for the waveform.



NOTES
1—The maximum allowable peak-to-peak ringing has to be less than 15% of I_{ps} with no observable ringing 100 ns after the start of the pulse.
2—Peak current (I_{ps}) shall be within 10% of the values specified in table 1. The actual values obtained have to be recorded for comparison with the I_{pr} values obtained with the 500 Ω resistor.

Figure 5—Current waveform through a short (T_{ds})



NOTES
1—The maximum allowable peak-to-peak ringing has to be less than 15% of I_{pr} with no observable ringing 100 ns after the start of the pulse.
2—Peak current shall be within 10% of the value specified in table 2 for I_{pr}. Also, it should not be less than 63% of the previously measured I_{ps} value for the same stress level.

Figure 6—Current waveform through a 500 Ω resistor

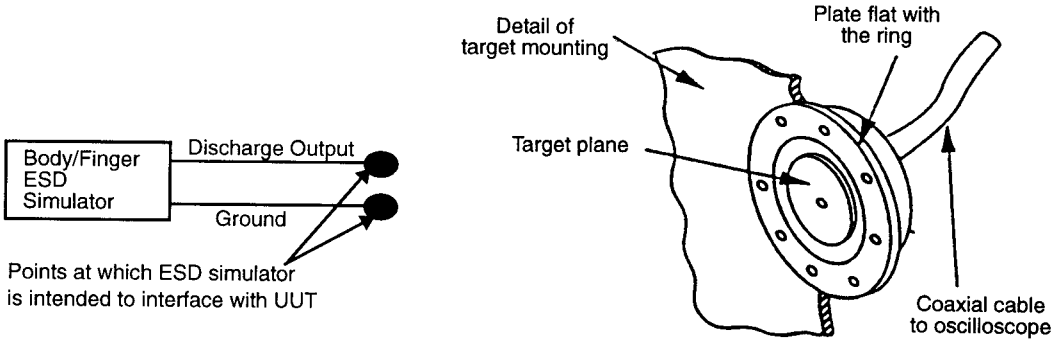
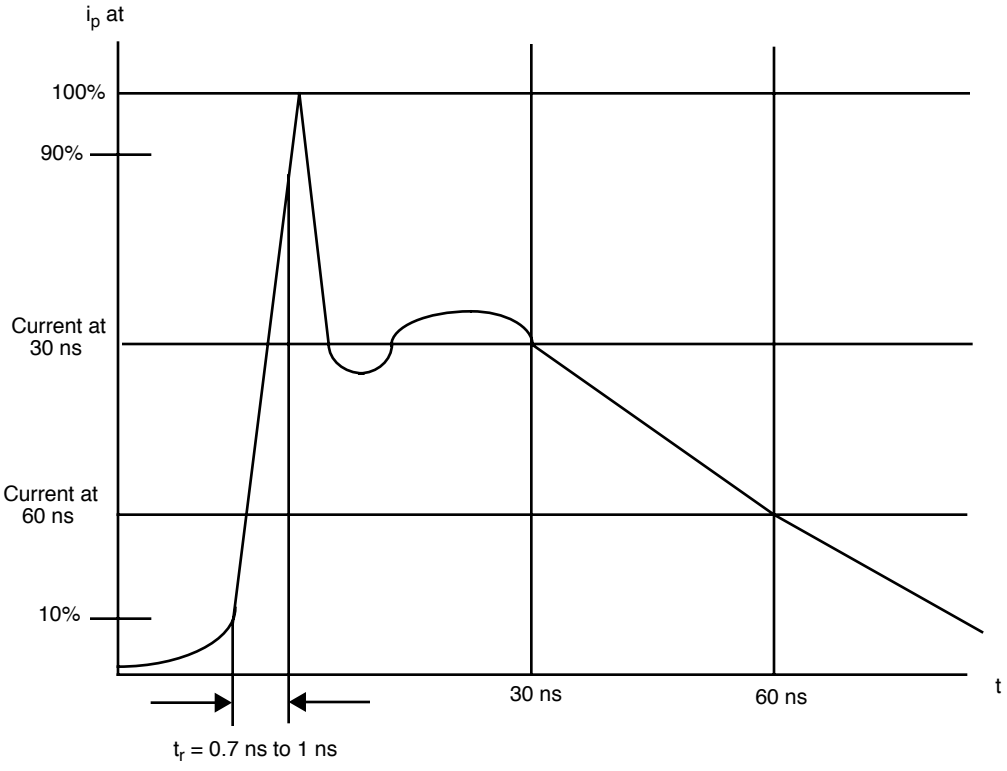


Figure 7—Waveform verification for hand/metal ESD simulator



t = time
t_r = risetime
I_p = peak current

Figure 8—Typical waveform of the output current of a hand/metal ESD simulator

Table 1—Verification parameters for a body/finger ESD waveform (into a short)

Equivalent peak voltage (V_p) (kV)	Peak current into a short (I_{ps}) ±10% (A)	Pulse risetime (T_{rs}) (ns)	Pulse decay time (T_{ds}) (ns)
0.5	0.33	2–10	150 ± 20
1.0	0.67	2–10	150 ± 20
2.0	1.33	2–10	150 ± 20
4.0	2.67	2–10	150 ± 20
6.0	4.00	2–10	150 ± 20
8.0	5.33	2–10	150 ± 20

Table 2—Verification parameters for a body/finger ESD waveform (into a 500 Ω resistor)

Equivalent peak voltage (V_p) (kV)	Peak current into a 500 Ω resistor with 0 pF (A)	Peak current into a 500 Ω resistor with 30 pF (A)	Pulse risetime (T_{rr}) (ns)	Pulse decay time (T_{rd}) (ns)
1.0	0.5	0.42	5–20	$1.4 \times T_{ds} \pm 20$

NOTE—The peak current into the 500 Ω resistor will vary depending upon the stray capacitive loading and peripheral wiring. The value shown in the 0 pF column represents the calculated value assuming zero capacitance. Values up to 30 pF are permissible, and the value of I_{pr} obtained with this maximum value of capacitance is shown under the column 30 pF. The *minimum* permitted I_{pr} is 63% of the actual I_{ps} level obtained for the same stress step. (Voltages above 1000 V may cause breakdown in resistors).

Table 3—Verification parameters for a hand/metal ESD waveform

Indicated voltage (kV)	First peak current of discharge ± 10% (A)	Risetime (t_r) with discharge switch (ns)	Current at 30 ns ± 30% (A)	Current at 60 ns ± 30% (A)
0.5	1.90	0.7–1.0	1	0.5
1.0	3.75	0.7–1.0	2	1.0
2.0	7.50	0.7–1.0	3	2.0
4.0	15.00	0.7–1.0	8	4.0
6.0	22.50	0.7–1.0	12	6.0
8.0	30.00	0.7–1.0	16	8.0

9. Bibliography

This is not a general bibliography on the subject of ESD, but is a specific bibliography relating to ESD testing of electronic subassemblies.

[B1] ANSI/EOS/ESD-S5.1-1993, Standard for Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBM) Component Level.

[B2] IEEE Std C62.47-1992, IEEE Guide on Electrostatic Discharge (ESD): Characterization of the ESD Voltage Environment (ANSI).

[B3] ISO Guide 45, Guidelines for the Presentation of Test Results.

[B4] MIL-STD 883D, *Test Methods and Procedures for Microelectronics*, Notice 8, Method 3015.7, "Electrostatic Discharge Sensitivity Classification."

[B5] Boxleitner, W., "ESD Stress on PCB Mounted ICs Caused by Charged Boards and Personnel," in *Proceedings of the EOS/ESD Symposium*, Sept. 10–13, 1990, pp. 54–60.

[B6] Lin, D. and Welsher, T., "ESD Stressing of Simulated Circuit Packs," in *Proceedings of the EOS/ESD Symposium*, Sept. 10–13, 1990, pp. 61–73.

[B7] Shaw, R. and Enoch, R., "An Experimental Investigation of ESD-Induced Damage to Integrated Circuits on Printed Circuit Boards," in *Proceedings of the EOS/ESD Symposium*, Sept. 10–12, 1985, pp. 132–140.

[B8] Weil, G., "Characterization and Test Methods for Printed Circuit Board ESD," in *Proceedings of the IEEE EMC Symposium*, Aug. 21–24, 1990, pp. 124–129.